

IN THE CLAIMS

Please amend the claims as follows:

1. (original) A logically partitioned data processing system, comprising:
 - a plurality of logical partitions;
 - a plurality of operating systems, each assigned to one of said plurality of logical partitions;
 - a plurality of memory locations, each location assigned to one of said plurality of logical partitions;
 - a data transmission bus;
 - at least one terminal bridge connected to said data transmission bus;
 - a plurality of input/output adapters, each associated with a different one of said plurality of logical partitions, said input/output adapters being connected to said terminal bridge; and
 - means for preventing transmission of data between a given one of said input/output adapters which is associated with a first one of the plurality of logical partitions, and memory locations unassigned to said first one of said plurality of logical partitions.
2. (original) The logically partitioned data processing system of Claim 1 wherein said data transmission bus is a PCI bus, and further comprising:
 - a PCI host bridge connected to said PCI bus; and
 - an input/output bus connected to said PCI host bridge.
3. (original) The logically partitioned data processing system of Claim 1 wherein said terminal bridge has a plurality of sets of range registers, each associated with a respective one of said input/output adapters.
4. (original) The logically partitioned data processing system of Claim 3 further comprising an arbiter which selects one of said input/output adapters to use said data transmission bus, wherein said transmission preventing means assigns one of said sets of range registers based on a grant signal from said arbiter.

5. (original) The logically partitioned data processing system of Claim 3 wherein said sets of range registers contain direct memory access addresses which limit operations that may be placed onto said data transmission bus by said input/output adapters.

6. (original) The logically partitioned data processing system of Claim 3 wherein said sets of range registers are programmable.

Claims 7-13 (canceled) ✓